IN THE SPECIFICATION

Please amend the specification at page 10, lines 11-26 as follows:

The half-rate phase detector of FIG. 4 generates the REF signal by means of third and fourth latches 430 and 432, which together comprise a second latch circuit that combines the first precursor signals Q1 and Q2 with alternate transitions of CLK2 to produce second precursor signals Q3 and Q4 from which the reference signal REF is derived. The latch 430 has a data input (D) connected to the output of the latch 415 via ~~417, 416~~ signal line 417 and inverter 416, a clock input for receiving the inverse form of CLK2, and an output (Q) connected via signal line 431 to the first input (I1) of a second XOR gate 434. The latch 432 has a data input (D) connected to the output of the latch 419 via ~~inverter~~ signal line 421 and ~~signal line~~ inverter 420, a clock input for receiving the positive form of CLK2, and an output (Q) connected via signal line 433 to the second input (I2) of the second XOR gate 434. The XOR gate 434 has an output (Q) connected to a signal line 435. As may be understood with reference to FIGS. 4 and 5, the latch 430 samples Q1 in response to the inverse form of CLK2 to produce Q3, and the latch 432 samples Q2 in response to the positive form of CLK2 to produce Q4. The precursor signal Q3 is combined with the precursor signal Q4 by an exclusive disjunction (exclusive-OR operation) performed by the XOR gate 434, which yields the reference signal.